Chapter II
RF/IF Components and
Specifications for Receivers

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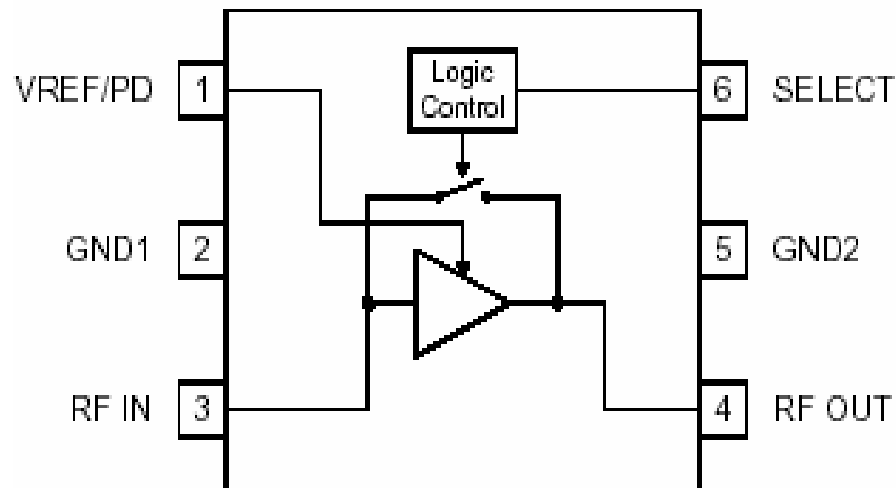DEVICES**

RF/IF Components and Specifications for Receivers

❑ **Fixed Gain and Variable Gain Amplifiers**

❑ **IQ Demodulators**

❑ **Analog-to-Digital Converters**
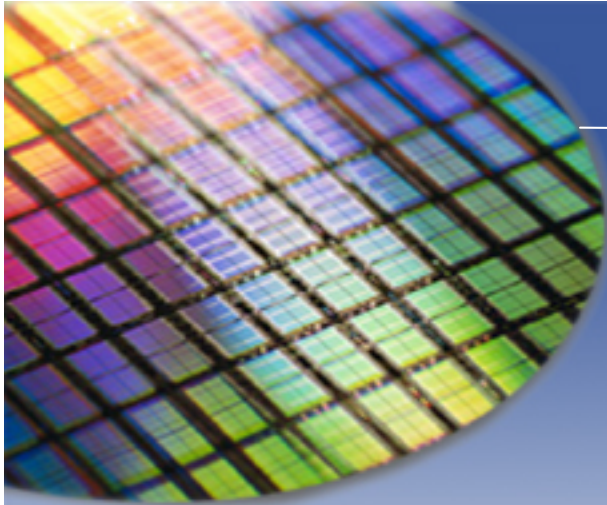
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Fixed Gain and Variable Gain Amplifiers

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RF Components – LNAs

VREF/PD [1] ⎯⎯ Logic Control ⎯⎯ [6] SELECT

GND1 [2] ⎯⎯ [5] GND2

RF IN [3] ⎯⎯ [4] RF OUT

- ❑ **Low Noise Amplifiers (LNA) amplify very small signals and add very little noise to the signal chain. Gain = 12-18 dB typically**
- ❑ **Noise Figure = 1-3 dB typically**
  - ❑ **A lower noise figure reduces overall system gain and power**
- ❑ **LNA must sometimes amplify a weak signal in the presence of a large blocker. So LNA must also have high IP3.**
- ❑ **Some LNAs have a bypass circuit which is engaged when the input signal is large**
- ❑ **LNAs are typically internally matched and specified for a narrow band of operation**
- ❑ **LNAs are often integrated with a receive mixer in portable applications**

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# AD8353 and AD8354 RF Gain Blocks
Silicon Bipolar 50 ohm input & output Gain Blocks

KEY SPECIFICATIONS

- ❑ Frequency Range: 1MHz to 2.7GHz
- ❑ P1dB: 9dBm   /   5dBm
- ❑ OIP3: 23dBm   /   19dBm
- ❑ NF: 5dB   /   4dB
- ❑ Isupply: 41mA   /   23mA
- ❑ Package: 3mm x 2mm 8-CSP

FEATURES

- ❑ Fully characterized over frequency range
- ❑ Fully characterized over temp –40 to +85 °C
- ❑ Output power stable over temperature <1dB
- ❑ Excellent gain stability over temp: < 1dB

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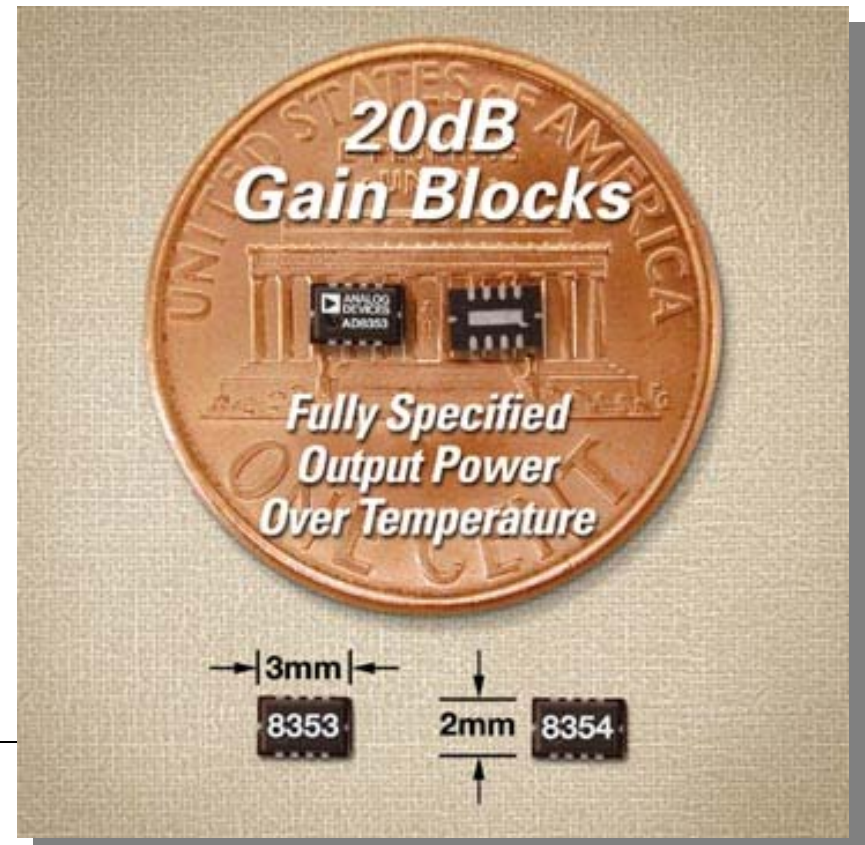
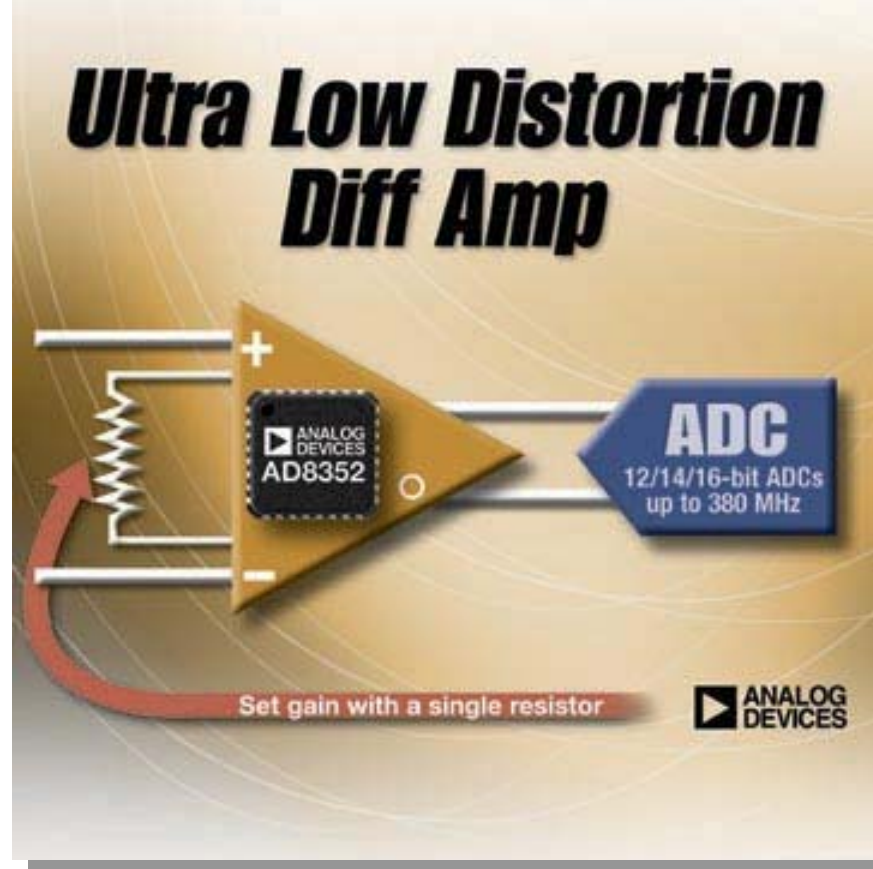# AD8352 – Lowest Distortion Differential Amplifier
Highest Performance Differential ADC Driver on the Market

KEY SPECIFICATIONS

❑ **Wide 3dB Bandwidth: 2GHz**

❑ **Low Distortion**

  ❑ **10 MHz, -86dBc HD2 -82dBc HD3**

  ❑ **70 MHz, -84dBc HD2 -82dBc HD3**

  ❑ **190Mhz, -81dBc HD2 -87dBc HD3**

❑ **High Linearity: Output IP3 +41dBm @ 150MHz**

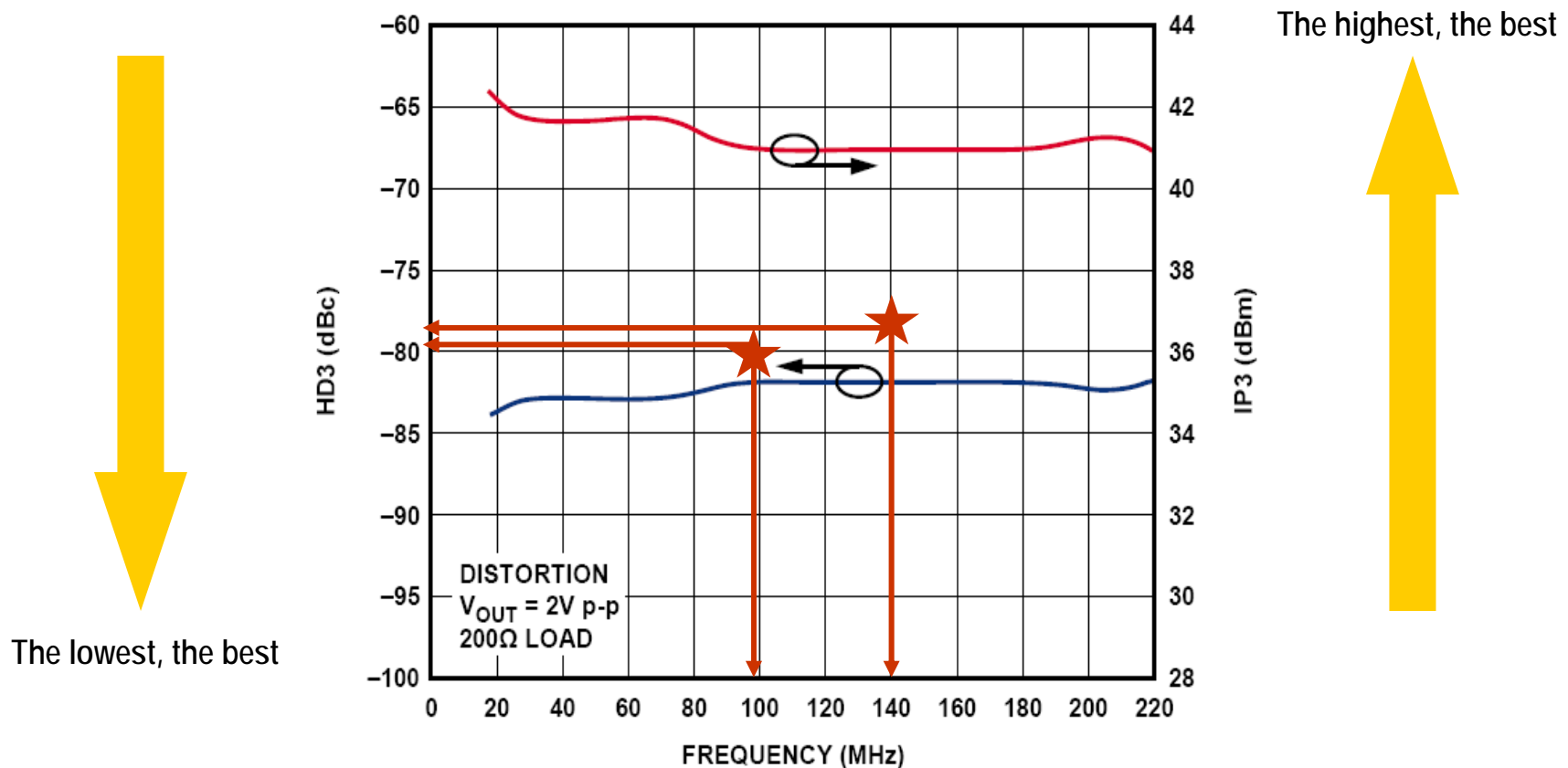❑ **Low Input Noise: 2.6nV/√Hz (Gain 10dB)**

FEATURES

❑ **Single Resistor sets Gain 3dB to 21dB**

❑ **Single Resistor & Capacitor distortion adjustment**
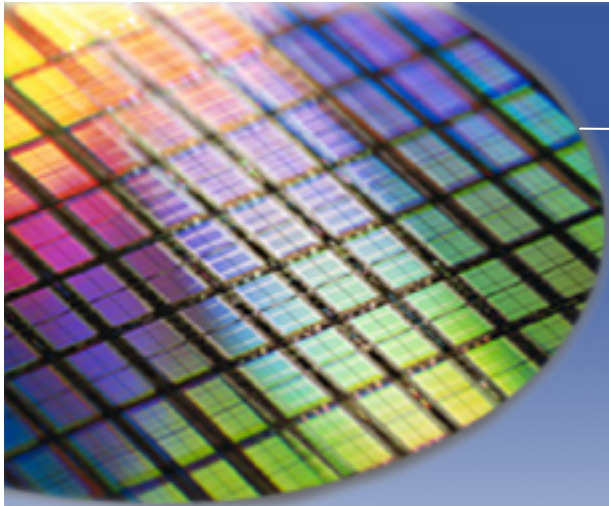
❑ **Small 3x3 mm 16-lead LFCSP**

Ultra Low Distortion Diff Amp

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AD8352

ADC
12/14/16-bit ADCs up to 380 MHz

Set gain with a single resistor

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AD8352 – Superior Distortion Specs
Lower Distortion @ Higher Frequencies

The highest, the best

The lowest, the best

★ Closest competition

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Receive VGAs

RF Components – Variable Gain Amplifiers

❑ In Receivers, VGAs adjust gain as received signal strength varies and present a constant signal level to the ADC

❑ In Transmitters, VGAs adjust for gain variations in the signal chain and set the output power to the desired level.

❑ Analog vs. Digital Control, Serial Control vs. Parallel Control – choice often depends on control interface that is available in the system.

❑ The AGC detector may be in DSP (after an ADC) or hardware or both
  ❑ a hardware AGC detector has a much faster response time
  ❑ A receiver with DSP-based AGC can be "blinded" by a strong signal while the system is responding

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AD8368 – RF/IF 800MHz Analog VGA

- ❏ **Features**
  - ❏ **Single ended 50Ω input / output**
  - ❏ **Analog Variable Gain Range: -11 to 22.5dB**
  - ❏ **Linear-in-dB Scaling: ~35dB/V**
  - ❏ **Integrated RMS AGC Detector**
  - ❏ **Single +5V supply**
  - ❏ **Small 4 x 4 mm 24-lead LFCSP**
- ❏ **Specifications**
  - ❏ **Wide 3dB Bandwidth: 800MHz**
  - ❏ **High Linearity Output IP3 +34dBm**
  - ❏ **High Output Compression P1dB: +16dBm**
  - ❏ **Low Noise Figure: 8dB max gain**
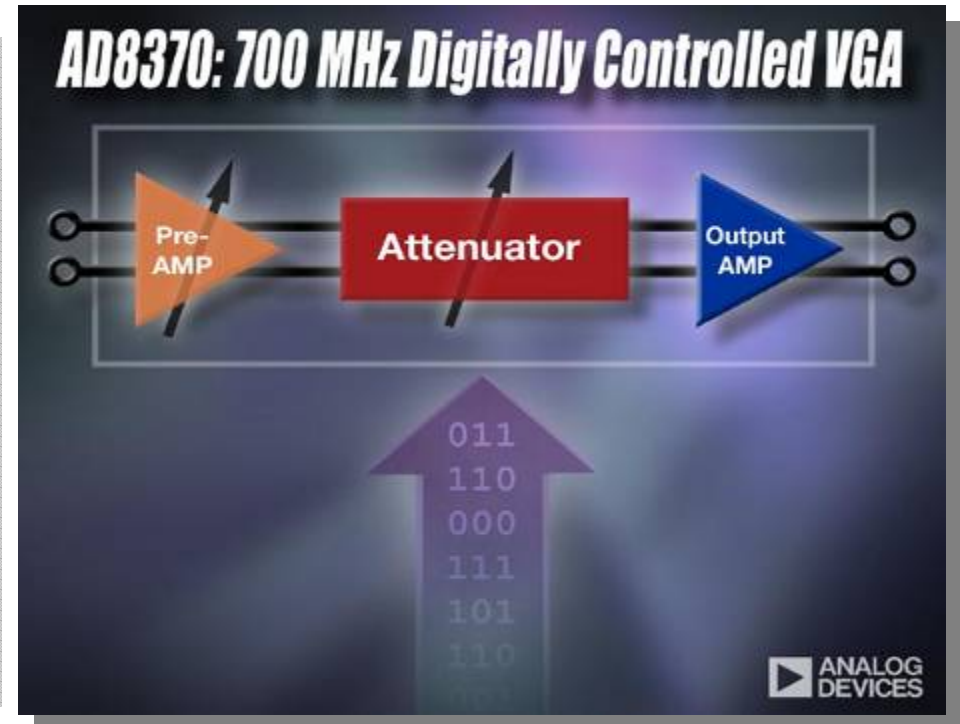

IF VGA Enables Complete AGC Loop

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AD8368

X^2

- On-chip *rms* power detector
- 34 dB linear-in-dB gain control

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AD8370 Fine Resolution DGA

KEY SPECIFICATIONS

❑ Bandwidth 750MHz

❑ Differential Input and Output Impedances:

   ❑ Zin = 200 Ω , Zout = 100Ω

❑ P1dB 17dBm (70Mhz)

❑ OIP3 35 dBm (70MHz) (1K load)

❑ OIP3 31dBm (70 MHz) (100 ohm load)

❑ Noise Figure 7dB (max gain)

❑ Package 16-TSSOP

AD8370: 700 MHz Digitally Controlled VGA

Pre-AMP — Attenuator — Output AMP

011
110
000
111
101
110

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FEATURES

❑ Serial 8-bit digital interface

❑ Wide gain control range

❑ Linear-in-dB Operation using Look Up Table

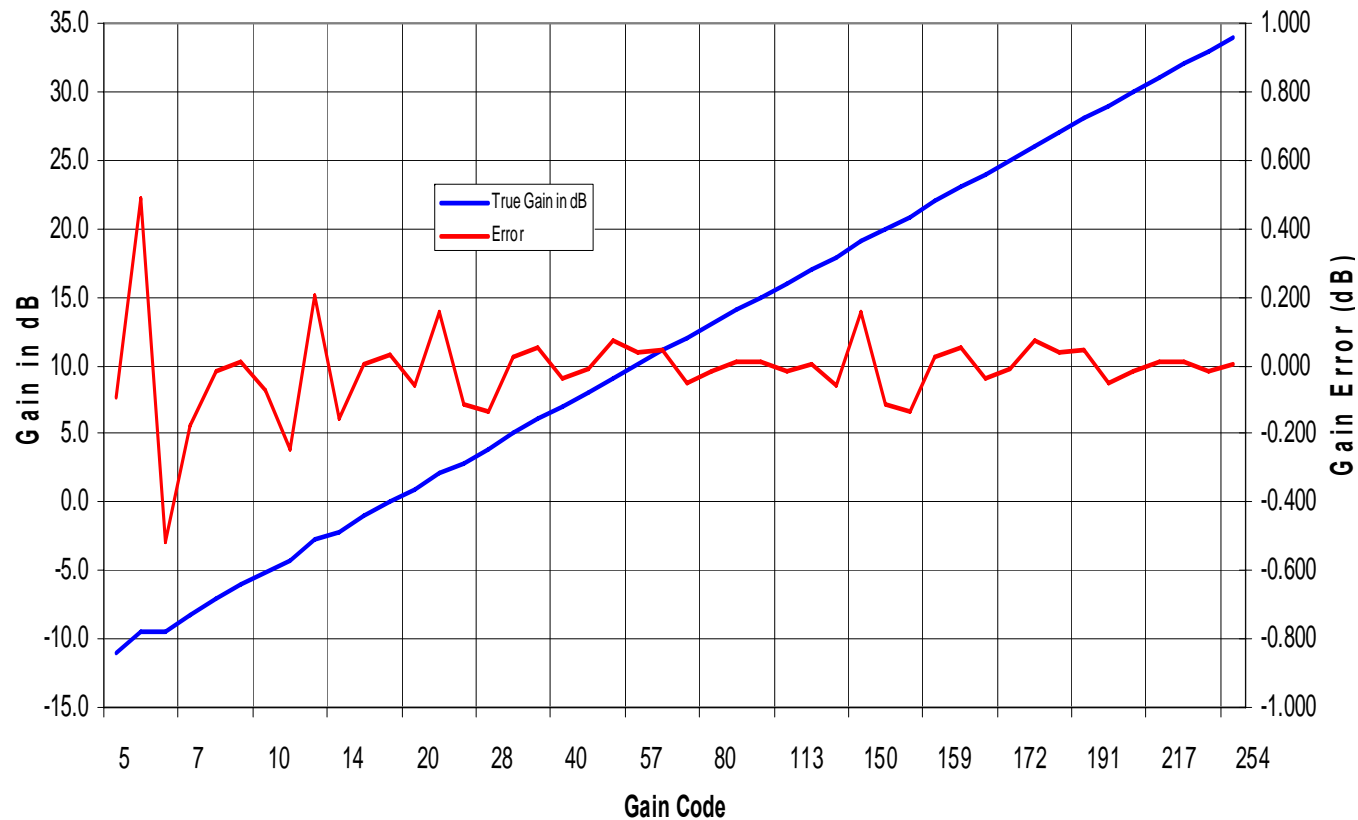❑ Power-down feature

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AD8370 Fine Resolution DGA: Gain Range
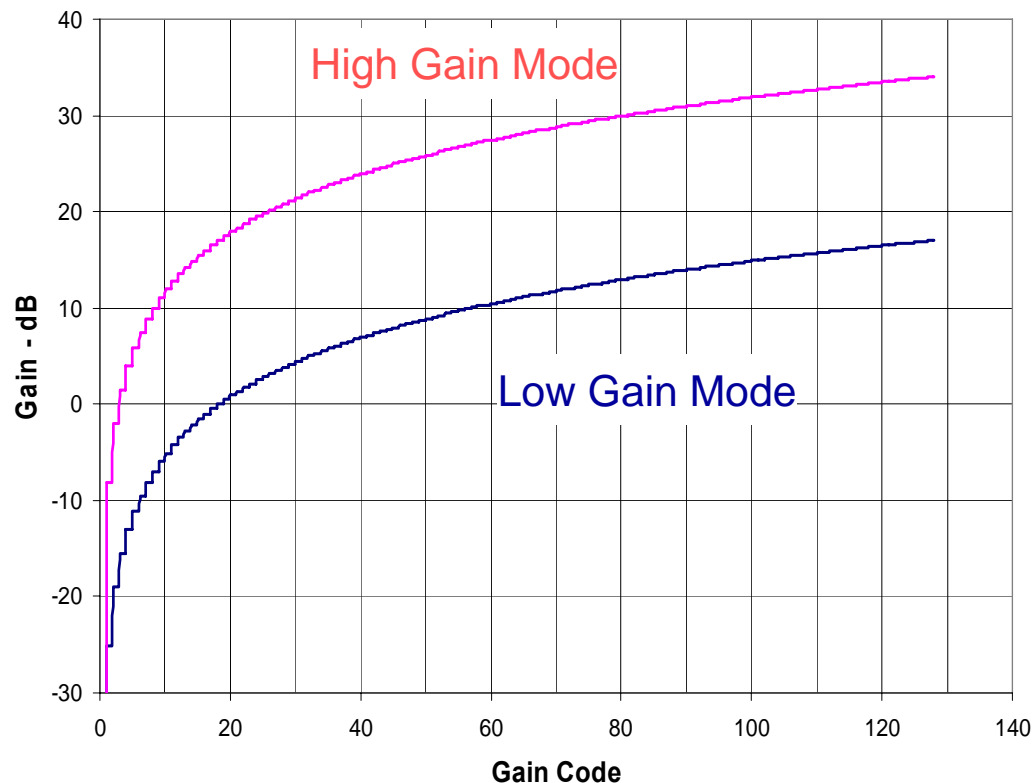
- **Two Operating Modes, High Gain and Low Gain, set by MSB Code**
- **Fine step size at the higher gain settings allows precise signal leveling**
- **Step size less than 1dB over-11 to 34dB gain range**

AD8370 DGA - Linear-in-dB Gain Code Mapping

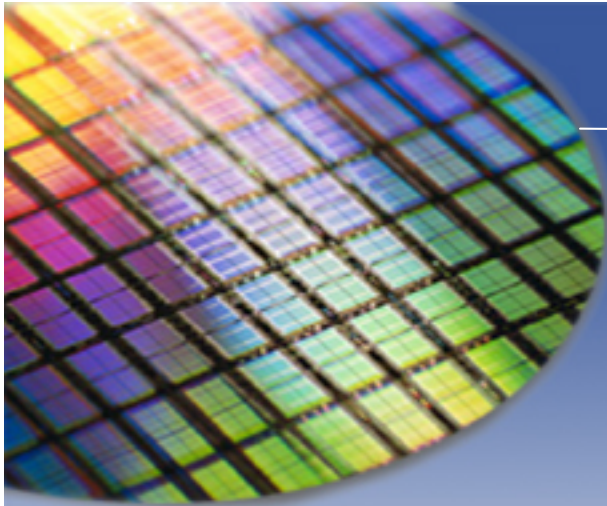Linear-in-dB Mapping of AD8370 Gain versus Gain Code

- **Gain Control can be made Linear-in-dB using simple look up table**

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Receive Amplifiers – Fixed Gain and Variable Gain

| Part No.	Control Type	Frequency Range (MHz)	Gain (dB)	Output IP3 (dBm)	Noise Figure (dB)	Comments
AD8367	Analog Variable	dc to 500	-2.5 to +42.5	27.5 (70MHz)	6.2	Single ended input/output
AD8368	Analog Variable	LF to 800	-11 to +22	34	8	Single ended input/output
AD8369	Digital Variable	LF to 600	-5 to +40	19.5 (70MHz)	7	Differential input/output
AD8370	Digital Variable	LF to 700	-11 to +17 +6 to +34	31 (70MHz)	7.4	Differential input/output
AD8350	Fixed Gain	LF-700	20	28	6.8	Differential ADC Driver
AD8351	Fixed Gain	LF-1000	26	33	9.5	Differential ADC Driver
AD8352	Fixed Gain	**LF - 2000**	**24**	**41**	**15.5**	Differential ADC Driver
AD8353	Fixed Gain	1 to 2700	20	23.6	5.3	Tx or Rx Gain Block
AD8354	Fixed Gain	1 to 2700	20	19	4.2	Tx or Rx Gain Block

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IQ Demodulators

RF Components – IQ Demodulators
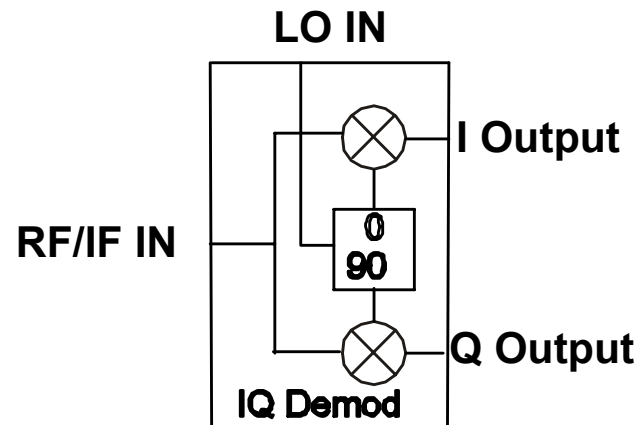
- ❑ **Reverse Function to IQ Modulator – IQ demodulation, extracts digital bits or symbols from a modulated carrier**
- ❑ **Local Oscillator (from PLL) at the same frequency as the center frequency of the carrier is split into "Quadrature" components of equal amplitude but 90 degrees out of phase**
- ❑ **Modulated signal is split and multiplied with Quadrature LO components (demodulation) to yield original IQ data/symbols**
- ❑ **For QPSK, digital data can be extracted using I and Q comparators**
- ❑ **For QAM, an ADC must be used to extract digital data**
- ❑ **Some IQ Demodulators have variable gain amplifiers at input and/or output**

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RF Components – IQ Demodulators

LO IN

RF IN

I Out

0
90
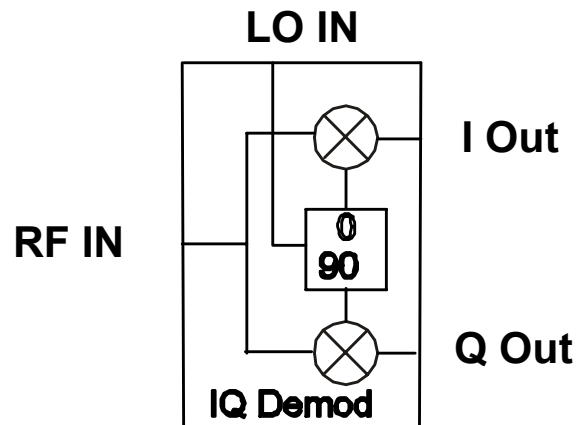
Q Out

IQ Demod

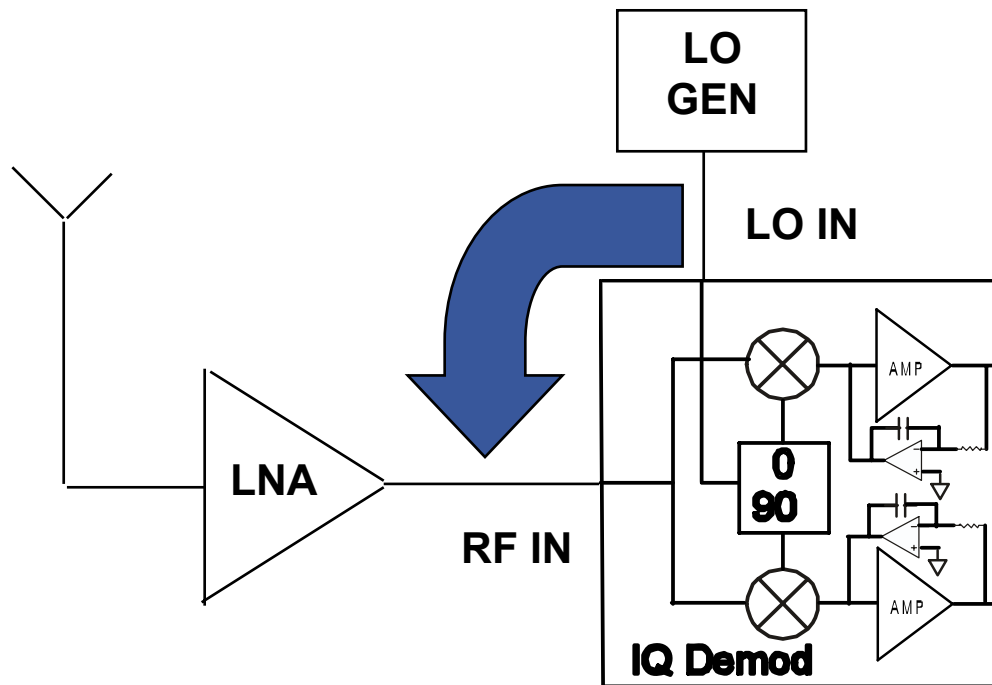❑ **Critical IQ Demodulator Specifications**
   ❑ **Noise Figure – determines achievable sensitivity of receiver**
   ❑ **Input IP3 – determines maximum acceptable input signal and/or blocker**
   ❑ **I and Q output bandwidth – determines maximum receivable bandwidth and symbol rate**
   ❑ **LO to RF leakage – generates output dc offsets which add to I and Q outputs**
   ❑ **Required LO Drive level – Lower LO input power results in less leakage**
   ❑ **IIP3 – low IIP3 can cause blockers to intermodulate and produce distortion at the carrier frequency, reducing receiver sensitivity**
   ❑ **IP2 – low IIP2 will cause RF Input to intermodulate with itself and produce unwanted dc offsets at output**

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LO to RF Leakage Causes Self-Mixing and DC Offset Voltages at I and Q Outputs

LO GEN

LO IN

I Out

DC Offsets

LNA

RF IN

0
90

Q Out
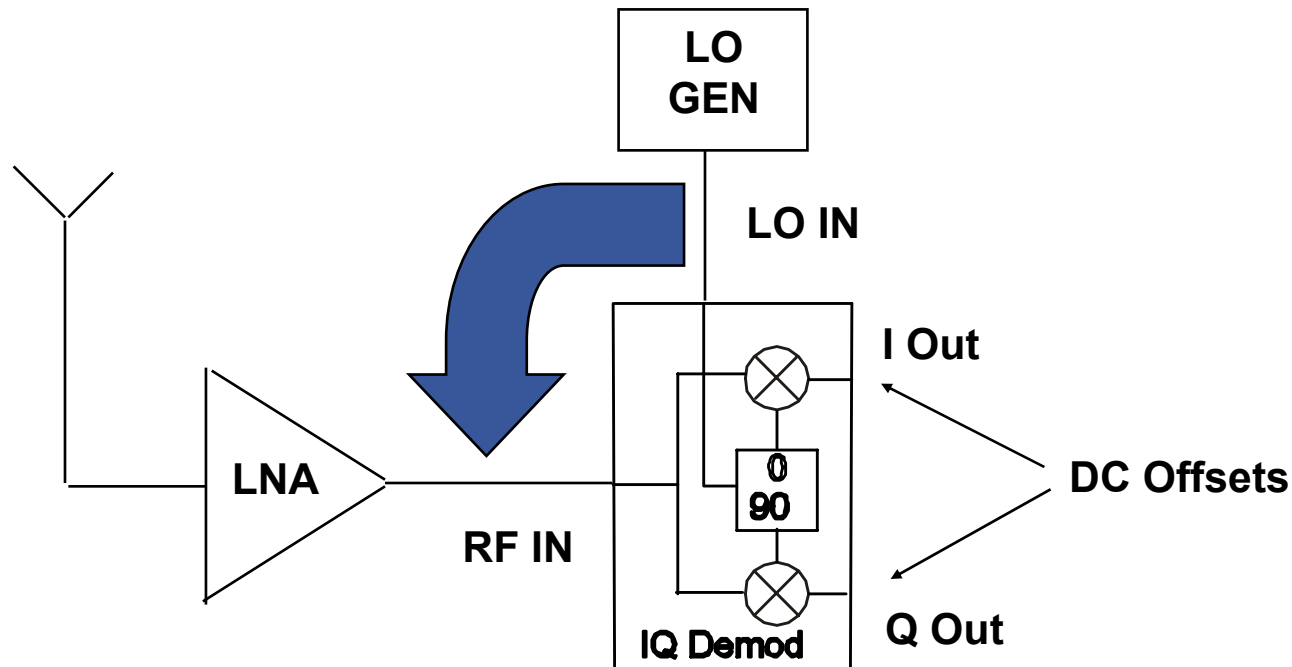
IQ Demod

❑ **Big Problem in Direct Conversion Receivers**
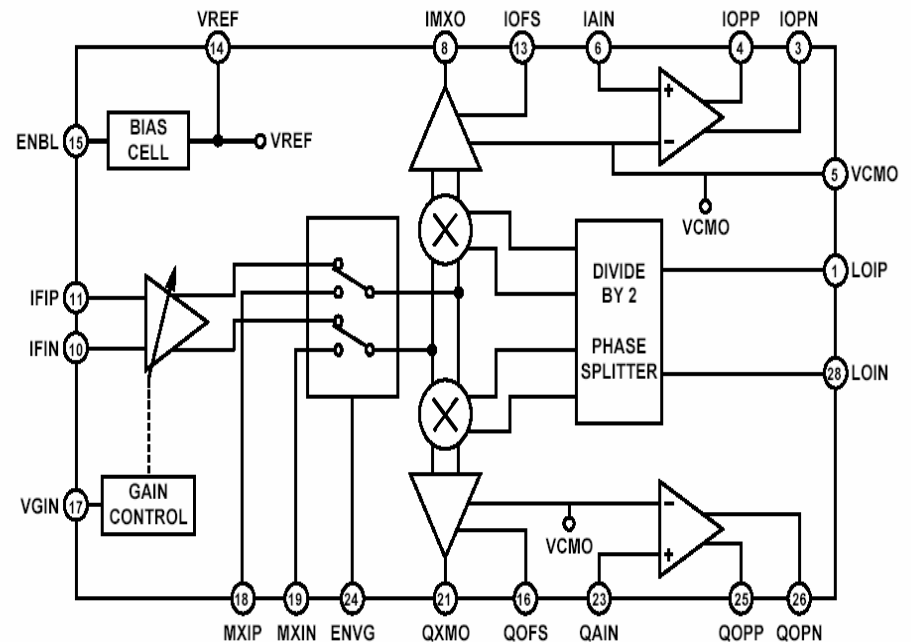
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Solution – Monitor and Null out DC Offsets at Baseband

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AD8348 I/Q Demodulator

KEY SPECIFICATIONS
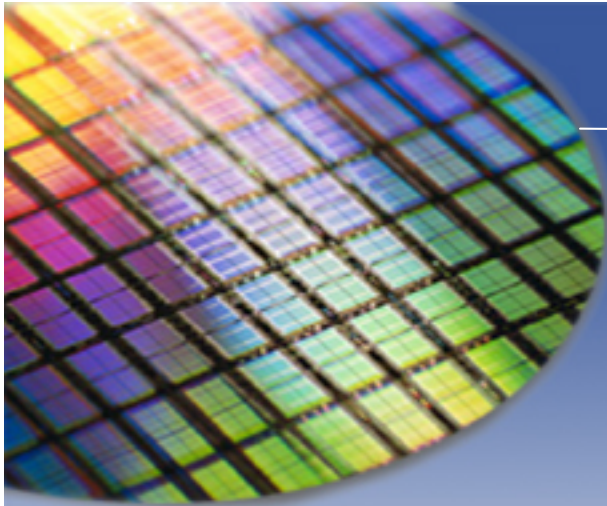
- Frequency Range 50MHz to 1000MHz
- Accuracy
  - Phase accuracy 0.5°
  - Amplitude balance 0.25 dB
- Demodulation bandwidth 75 MHz
- IIP3 +28 dBm @ min gain
- IIP3 –8 dBm @ max gain
- Amplitude balance 0.25 dB
- Noise figure 11 dB @ max gain
- Package 28-lead TSSOP

FEATURES

- Integrated I/Q demodulator with IF VGA amplifier
- Linear-in-dB AGC range 44 dB
- Power-Down Mode
- Integrated DC offset-nulling

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ADCs

RF Components – ADCs

❑ **Baseband ADCs (usually sold as duals) sample QAM outputs from an IQ demodulator.**

    ❑ **Higher order modulation schemes** $\rightarrow$ **higher resolution ADCs**

    ❑ **Higher ADC resolution** $\rightarrow$ **lower noise** $\rightarrow$ **increased sensitivity**

    ❑ **Higher symbol rates** $\rightarrow$ **higher ADC sampling rates**

❑ **IF Sampling ADCs capture signal at Intermediate Frequency and mix it down into the first Nyquist band.**

    ❑ **Require high input (analog) bandwidth**

    ❑ **typically more expensive than baseband ADCs**

    ❑ **eliminate down conversion analog circuitry (PLL, Mixer)**

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